Radiation Hardened Ultra Low Noise, Precision Voltage Reference

ISL71090SEH25

The ISL71090SEH25 is an ultra low noise, high DC accuracy precision voltage reference with a wide input voltage range from 4V to 30V. The ISL71090SEH25 uses the Intersil Advanced Bipolar technology to achieve sub 2µV_{P-P} noise at 0.1Hz with an accuracy over temperature of 0.15%.

The ISL71090SEH25 offers a 2.5V output voltage with 10ppm/°C temperature coefficient and also provides excellent line and load regulation. The device is offered in an 8 Ld Flatpack package.

The ISL71090SEH25 is ideal for high-end instrumentation, data acquisition and applications requiring high DC precision where low noise performance is critical.

Applications

- RH voltage regulators precision outputs
- Precision voltage sources for data acquisition system for space applications
- Strain and pressure gauge for space applications

Features

- **Reference output voltage . . . . 2.5V ±0.05%**
- **Accuracy over temperature . . . . ±0.15%**
- **Output voltage noise . . . . 2µV_{P-P} Typ (0.1Hz to 10Hz)**
- **Voltage accuracy over radiation . . . . ±0.175%**
- Supply current . . . . 930µA (Typ)
- Tempco (box method) . . . . 10ppm/°C Max
- Output current capability 20mA
- Line regulation 8ppm/V
- Load regulation 2.5ppm/mA
- Operating temperature range. . . . .-55°C to +125°C
- **Radiation environment**
  - **High dose rate (50-300rad(Si)/s) . . . . 100krad(Si)**
  - **Low dose rate (0.01rad(Si)/s) . . . . .100krad(Si)***
  - **SET/SEL/SEB . . . . 86MeV•cm^2/mg**

*Product capability established by initial characterization. The "EH" version is acceptance tested on a wafer by wafer basis to 50krad(Si) at low dose rate

- Electrically screened to SMD 5962-13211

Related Literature

- AN1847, "ISL71090SEHXX Evaluation Board User's Guide"
- AN1848, "SEE Testing of the ISL71090SEHXX"
- AN1849, "Radiation Report of the ISL71090SEHXX"

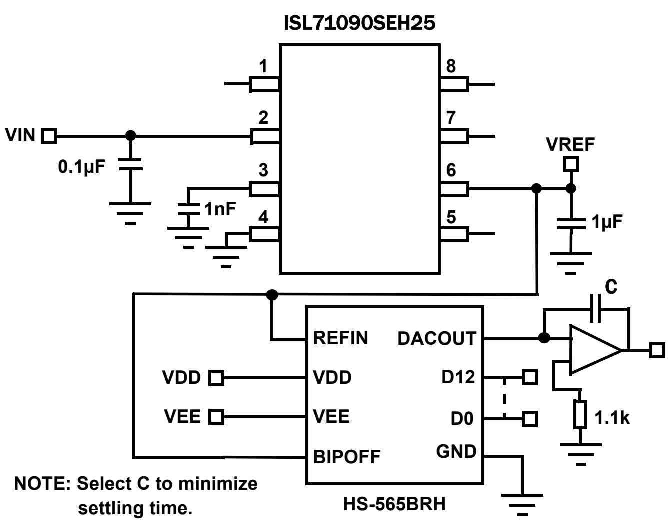


FIGURE 1. ISL71090SEH25 TYPICAL APPLICATION DIAGRAM

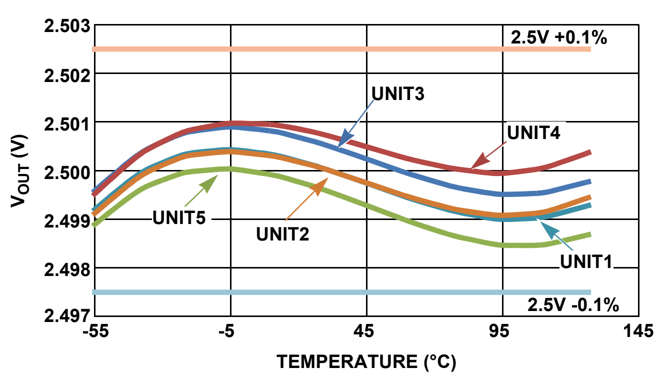


FIGURE 2. V_{OUT} vs TEMPERATURE

Ordering Information

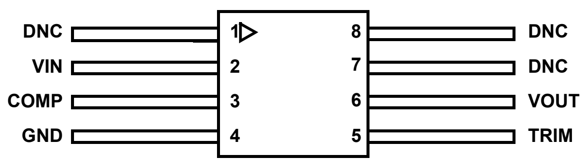
ORDERING NUMBER (Notes 1, 2)	PART NUMBER	V_{OUT} OPTION (V)	TEMP RANGE (°C)	PACKAGE TAPE & REEL (Pb-Free)	PKG. DWG. #
5962R1321102VXC	ISL71090SEHVF25	2.50	-55 to +125	8 Ld Flatpack	K8.A
ISL71090SEHF25/PROTO	ISL71090SEHF25/PROTO	2.50	-55 to +125	8 Ld Flatpack	K8.A
5962R1321102V9A	ISL71090SEHVX25	2.50	-55 to +125	Die	
ISL71090SEHX25SAMPLE	ISL71090SEHX25SAMPLE	2.50	-55 to +125	Die	
ISL71090SEHF25EVAL1Z	Evaluation Board				

NOTES:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in this “Ordering Information” table must be used when ordering.

Pin Configuration

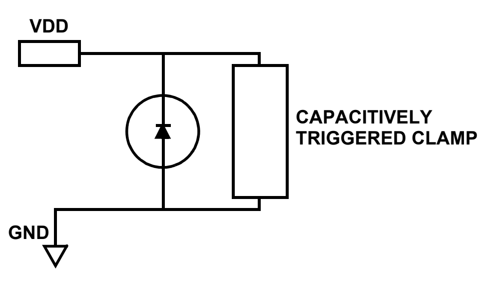
ISL71090SEH25
(8 LD FLATPACK)
TOP VIEW



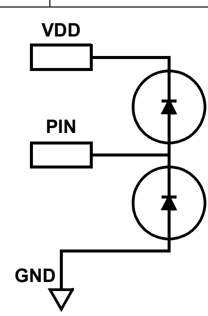
NOTE: The ESD triangular mark is indicative of pin #1. It is a part of the device marking and is placed on the lid in the quadrant where pin #1 is located.

Pin Description

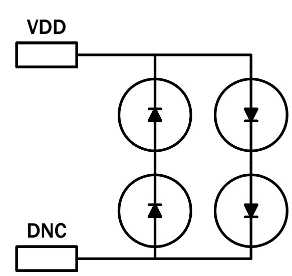
PIN NUMBER	PIN NAME	ESD CIRCUIT	DESCRIPTION
1, 7, 8	DNC	3	Do not Connect. Internally Terminated.
2	VIN	1	Input Voltage Connection
3	COMP	2	Compensation and Noise Reduction Capacitor
4	GND	1	Ground Connection. Also connected to the lid.
5	TRIM	2	Voltage Reference Trim input
6	VOUT	2	Voltage Reference Output



ESD CIRCUIT 1

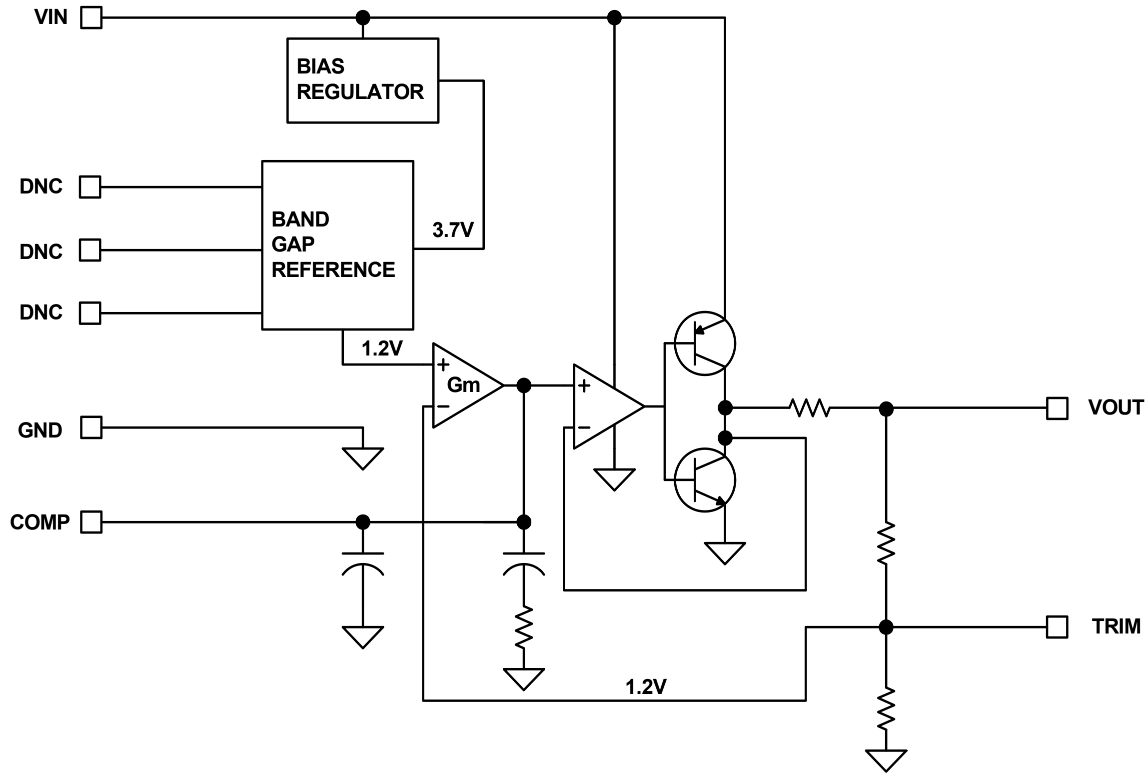


ESD CIRCUIT 2



ESD CIRCUIT 3

Functional Block Diagram



Absolute Maximum Ratings

Max Voltage
V_{IN} to GND . . . . . -0.5V to +40V
V_{IN} to GND at an LET = 86MeV•cm^2/mg . . . . . -0.5V to +36V
V_{OUT} to GND (10s) . . . . . -0.5V to V_{OUT} + 0.5V
Voltage on any Pin to Ground . . . . . -0.5V to +V_{OUT} + 0.5V
Voltage on DNC Pins . . . . . No connections permitted to these pins
Input Voltage Slew Rate (Max) 0.1V/µs
ESD Ratings
Human Body Model 2kV
Machine Model 200V
Charged Device Model 750V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld Flatpack Package (Notes 3, 4)	140	15

Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature (T_{JMAX}) . . . . . +150°C
Pb-Free Reflow Profile (Note 5) . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

V_{IN} . . . . . 4.0V to +30V
Temperature Range . . . . . -55°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. For θ_{JC}, the "case temp" location is the center of the ceramic on the package underside.
5. Post-reflow drift for the ISL71090SEH25 devices can be 100µV typical based on experimental results with devices on FR4 double sided boards. The engineer must take this into account when considering the reference voltage after assembly.
6. Product capability established by initial characterization. The "EH" version is acceptance tested on a wafer by wafer basis to 50krad(Si) at low dose rate.
7. The output capacitance used for SEE testing is 0.1µF for C_{IN} and C_{OUT}.

Electrical Specifications For Flatpack

V_{IN} = 5V, I_{OUT} = 0mA, C_{OUT} = 0.1µF, COMP = 1nF unless otherwise specified. **Boldface limits apply over the operating temperature range, -55°C to +125°C and radiation.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
V_{OUT}	Output Voltage			2.5		V
V_{OA}	V_{OUT} Accuracy @ T_A = +25°C (Note 5)	V_{OUT} = 2.5V	-0.05		+0.05	%
V_{OA}	V_{OUT} Accuracy @ T_A = -55°C to +125°C	V_{OUT} = 2.5V	**-0.15**		**+0.15**	%
V_{OA}	V_{OUT} Accuracy @ T_A = -55°C to +125°C, Post Rad	V_{OUT} = 2.5V	-0.175		+0.175	%
TC V_{OUT}	Output Voltage Temperature Coefficient (Note 9)				**10**	ppm/°C
V_{IN}	Input Voltage Range		**4**		**30**	V
I_{IN}	Supply Current			0.930	**1.28**	mA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 4V to 30V		8	**18**	ppm/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	Sourcing: 0mA ≤ I_{OUT} ≤ 20mA		20	**35**	ppm/mA
		Sinking: -10mA ≤ I_{OUT} ≤ 0mA		40	**70**	ppm/mA
V_D	Dropout Voltage (Note 10)	I_{OUT} = 10mA		1.1	**1.7**	V
I_{SC+}	Short Circuit Current	T_A = +25°C, V_{OUT} tied to GND		55		mA
I_{SC-}	Short Circuit Current	T_A = +25°C, V_{OUT} tied to V_{IN}		-61		mA
t_R	Turn-on Settling Time	90% of final value, C_L = 1.0µF, C_C = open		150		µs
	Ripple Rejection	f = 120Hz		90		dB
e_N	Output Voltage Noise	0.1Hz ≤ f ≤ 10Hz		1.9		μV_{P-P}
V_N	Broadband Voltage Noise	10Hz ≤ f ≤ 1kHz		1.6		μV_{RMS}
	Noise Density	f = 1kHz		50		nV/√Hz
$\Delta V_{OUT}/\Delta t$	Long Term Drift	T_A = +125°C, 1000Hrs		15		ppm

Electrical Specifications For Die

V_{IN} = 5V, I_{OUT} = 0mA, C_{OUT} = 0.1µF, COMP = 1nF unless otherwise specified. **Boldface limits apply over the operating temperature range, -55°C to +125°C and radiation.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
V_{OUT}	Output Voltage (Note 11)			2.5		V
V_{OA}	V_{OUT} Accuracy @ T_A = +25°C (Note 5)	V_{OUT} = 2.5V	-0.05		+0.05	%
V_{OA}	V_{OUT} Accuracy @ T_A = -55°C to +125°C	V_{OUT} = 2.5V	**-0.15**		**+0.15**	%
V_{OA}	V_{OUT} Accuracy @ T_A = -55°C to +125°C, Post Rad	V_{OUT} = 2.5V	-0.175		+0.175	%
TC V_{OUT}	Output Voltage Temperature Coefficient (Note 9)				**10**	ppm/°C
V_{IN}	Input Voltage Range		**4**		**30**	V
I_{IN}	Supply Current			0.930	**1.28**	mA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 4V to 30V		8	**18**	ppm/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	Sourcing: 0mA ≤ I_{OUT} ≤ 20mA		20	**35**	ppm/mA
		Sinking: -10mA ≤ I_{OUT} ≤ 0mA		40	**70**	ppm/mA
V_D	Dropout Voltage (Note 10)	I_{OUT} = 10mA		1.1	**1.7**	V

NOTES:

8. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
9. Over the specified temperature range. Temperature coefficient is measured by the box method whereby the change in V_{OUT} is divided by the temperature range; in this case, -55°C to +125°C = +180°C.
10. Dropout Voltage is the minimum V_{IN} - V_{OUT} differential voltage measured at the point where V_{OUT} drops 1mV from V_{IN} = nominal at T_A = +25°C.
11. The VOUT accuracy is based on die mount with Silver Glass die attach material such as "QMI 2569" or equivalent in a package with an Alumina ceramic substrate

Typical Performance Curves
V_{IN} = 5V, V_{OUT} = 2.5V, T_A = +25°C, C_{OUT} = 0.1µF, COMP = 1nF unless otherwise specified.

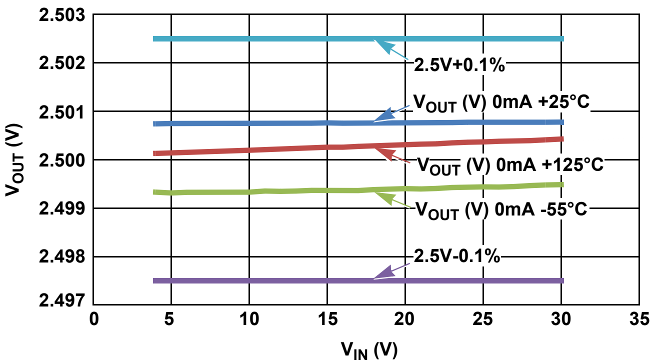


FIGURE 3. V_{OUT} ACCURACY OVER-TEMPERATURE

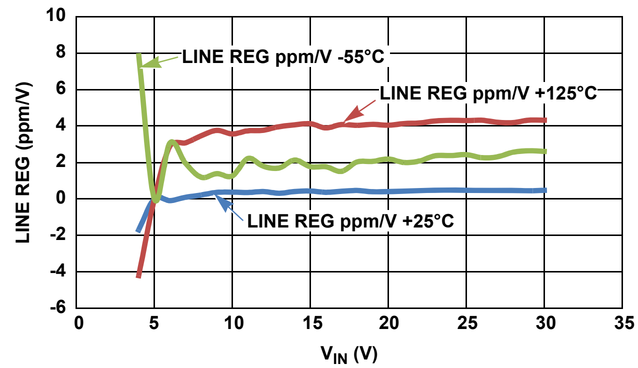


FIGURE 4. LINE REGULATION OVER-TEMPERATURE (0mA)

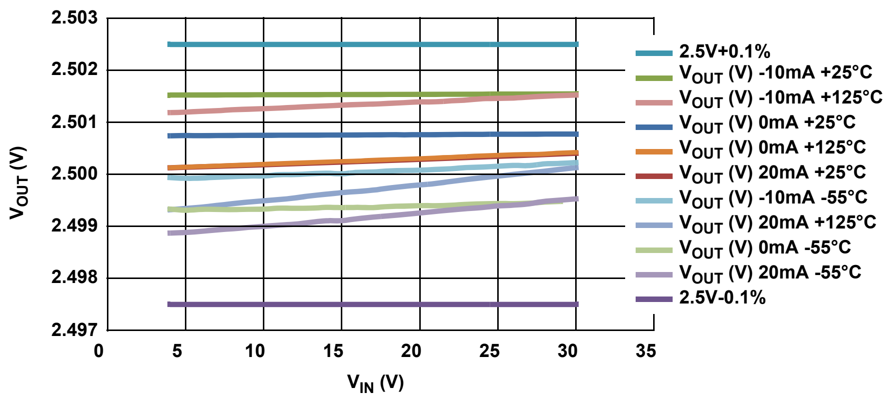


FIGURE 5. V_{OUT} vs V_{IN} AT 0mA, 20mA AND -10mA

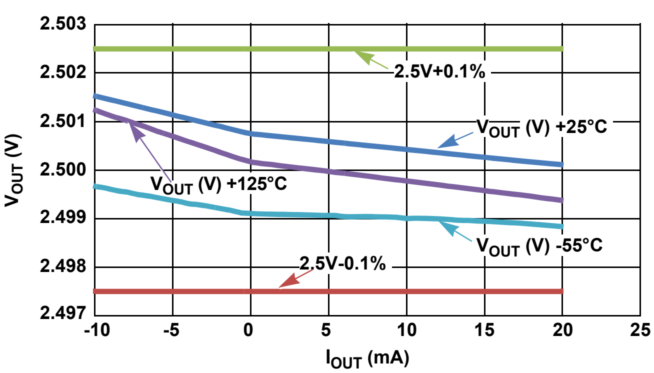


FIGURE 6. LOAD REGULATION OVER-TEMPERATURE AT V_{IN} = 5V (V)

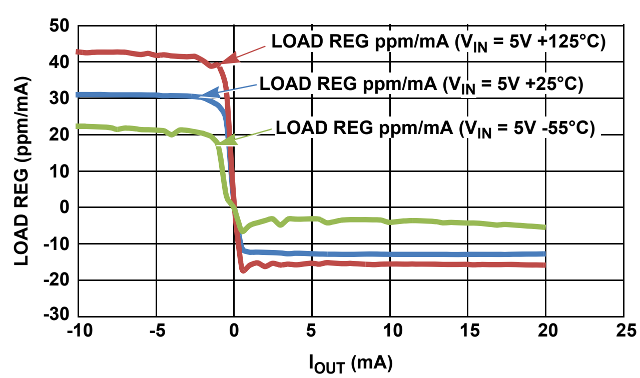


FIGURE 7. LOAD REGULATION OVER-TEMPERATURE AT V_{IN} = 5V (ppm/mA)

Typical Performance Curves V_{IN} = 5V, V_{OUT} = 2.5V, T_A = +25°C, C_{OUT} = 0.1µF, COMP = 1nF unless otherwise specified.

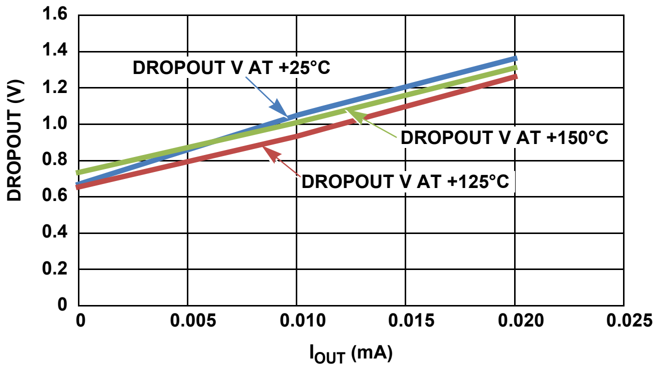


FIGURE 8. DROPOUT VOLTAGE FOR 2.5V

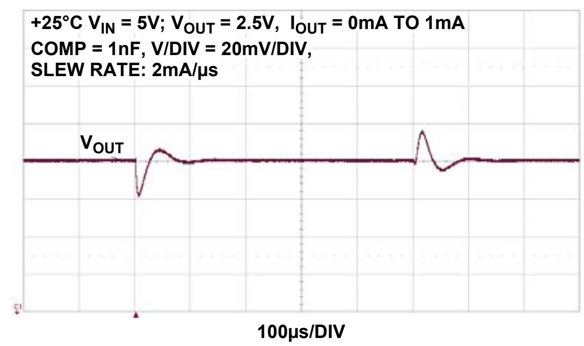


FIGURE 9. LOAD TRANSIENT (0mA TO 1mA)

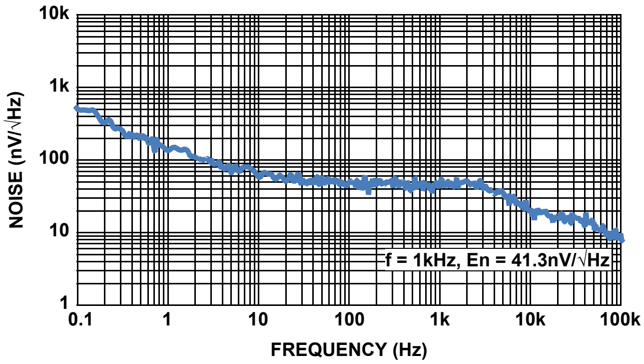


FIGURE 10. NOISE DENSITY vs FREQUENCY (V_{IN} = 5.0V, I_{OUT} = 0mA, C_{IN} = 0.1µF, C_{OUT} = 1µF, COMP = 1nF)

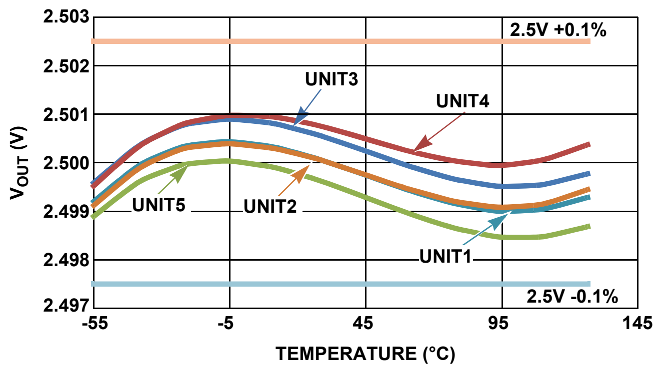


FIGURE 11. TYPICAL TEMPERATURE COEFFICIENT PLOT FOR 5 UNITS

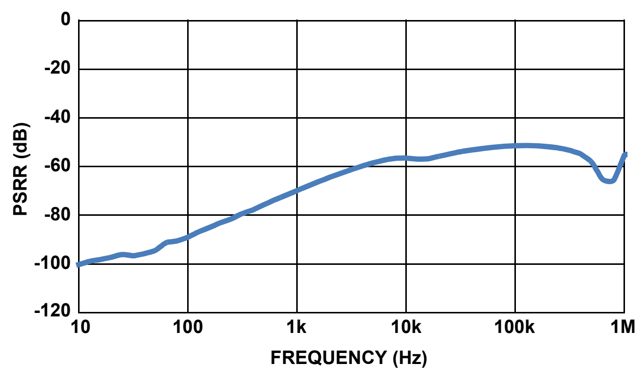


FIGURE 12. PSRR (+25°C, V_{IN} = 5V, V_{OUT} = 2.5V, I_{OUT} = 0mA, C_{IN} = C_{OUT} = 0.1µF, COMP = 1nF, VSIG = 300mV_{P-P})

Device Operation

Bandgap Precision Reference

The ISL71090SEH25 uses a bandgap architecture and special trimming circuitry to produce a temperature compensated, precision voltage reference with high input voltage capability and moderate output current drive.

Applications Information

Board Mounting Considerations

For applications requiring the highest accuracy, board mounting location should be reviewed. The device uses a ceramic flatpack package. Generally, mild stresses to the die when the printed circuit (PC) board is heated and cooled, can slightly change the shape. Because of these die stresses, placing the device in areas subject to slight twisting can cause degradation of reference voltage accuracy. It is normally best to place the device near the edge of a board, or on the shortest side, because the axis of bending is most limited in that location. Mounting the device in a cutout also minimizes flex. Obviously, mounting the device on flexprint or extremely thin PC material will likewise cause loss of reference accuracy.

Board Assembly Considerations

Some PC board assembly precautions are necessary. Normal output voltage shifts of typically 100µV can be expected with Pb-free reflow profiles or wave solder on multi-layer FR4 PC boards. Precautions should be taken to avoid excessive heat or extended exposure to high reflow or wave solder temperatures.

Noise Performance and Reduction

The output noise voltage over the 0.1Hz to 10Hz bandwidth is typically 2µV_{P-P} (V_{OUT} = 2.5V). The noise measurement is made with a 9.9Hz bandpass filter. Noise in the 10Hz to 1kHz bandwidth is approximately 1.6µV_{RMS} (V_{OUT} = 2.5V), with 0.1µF capacitance on the output. This noise measurement is made with a band pass filter of 990Hz. Load capacitance up to 10µF (with COMP) can be added but will result in only marginal improvements in output noise and transient response.

Turn-On Time

Normal turn-on time is typically 150µs, the circuit designer must take this into account when looking at power-up delays or sequencing.

Temperature Coefficient

The limits stated for temperature coefficient (Tempco) are governed by the method of measurement. The overwhelming standard for specifying the temperature drift of a reference is to measure the reference voltage at two temperatures which provide for the maximum voltage deviation and take the total variation, (V_{HIGH} - V_{LOW}), this is then divided by the temperature extremes of measurement (T_{HIGH} – T_{LOW}). The result is divided by the nominal reference voltage (at T = +25°C) and multiplied by 10^6 to yield ppm/°C. This is the “Box” method for specifying temperature coefficient.

Output Voltage Adjustment

The output voltage can be adjusted above and below the factory-calibrated value via the trim terminal. The trim terminal is the negative feedback divider point of the output op amp. The positive input of the amplifier is about 1.216V, and in feedback, so will be the trim voltage. The suggested method to adjust the output is to connect a 1MΩ external resistor directly to the trim terminal and connect the other end to the wiper of a potentiometer that has a 100kΩ resistance and whose outer terminals connect to V_{OUT} and ground. If a 1MΩ resistor is connected to trim, the output adjust range will be ±6.3mV. The TRIM pin should not have any capacitor tied to its output, also it is important to minimize the capacitance on the trim terminal during layout to preserve output amplifier stability. It is also best to connect the series resistor directly to the trim terminal, to minimize that capacitance and also to minimize noise injection. Small trim adjustments will not disturb the factory-set temperature coefficient of the reference, but trimming near the extreme values can.

Output Stage

The output stage of the device has a push-pull configuration with a high-side PNP and a low-side NPN. This helps the device to act as a source and sink. The device can source 20mA and sink 10mA.

Use of COMP Cap

The reference can be compensated for the C_{OUT} capacitors used by adding a capacitor from COMP pin to GND. See Table 1 for recommended values. of the COMP capacitor.

TABLE 1.

C_{OUT} (µF)	C_{COMP} (nF)
0.1	1
1	1
10	10

SEE Testing

The device was tested under ion beam at an LET of 86MeV • cm^2/mg. The device did not latch-up or burn out to a VDD of 36V and at +125°C. Single Event transients were observed and are summarized in the Table 2:

TABLE 2.

V_{IN} (V)	I_{OUT} (mA)	C_{OUT} (µF)	SET (% V_{OUT})
4	5	1	-4.6
30	5	1	-4.4
30	5	10	-1.0

DNC Pins

These pins are for trimming purpose and for factory use only. Do not connect these to the circuit in any way. It will adversely effect the performance of the reference.

Package Characteristics

Weight of Packaged Device

0. 31 Grams (Typical)

Lid Characteristics

Finish: Gold
Potential: Connected to pin #4 (GND)
Case Isolation to Any Lead: 20 x 10^9 Ω (min)

Die Characteristics

Die Dimensions

1464µm x 1744µm (58mils x 69mils)
Thickness: 483µm ± 25µm (19mils ± 1 mil)

Interface Materials

GLASSIVATION

Type: Nitrox
Thickness: 15kÅ

TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
Thickness: 30kÅ

BACKSIDE FINISH

Silicon

ASSEMBLY RELATED INFORMATION

SUBSTRATE POTENTIAL

Floating

ADDITIONAL INFORMATION

WORST CASE CURRENT DENSITY

<2 x 10^5 A/cm^2

PROCESS

Dielectrically Isolated Advanced Bipolar Technology- PR40

Metallization Mask Layout

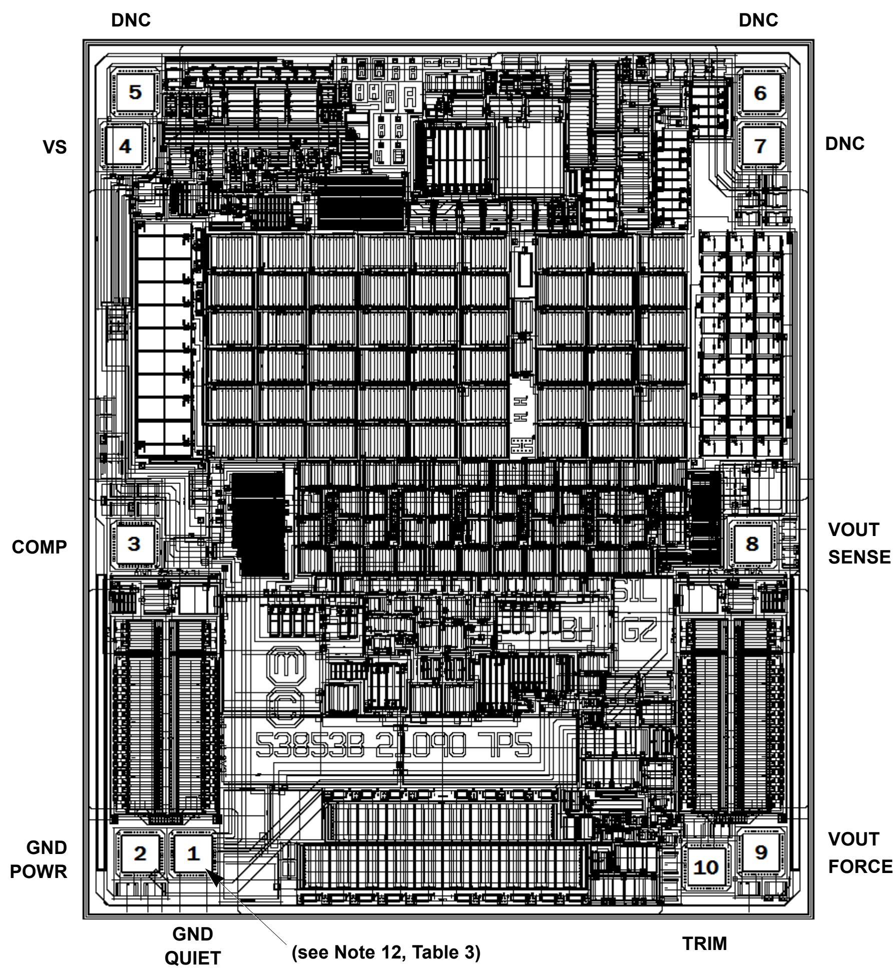


TABLE 3. DIE LAYOUT X-Y COORDINATES

PAD NAME	PAD NUMBER	X (µm)	Y (µm)	BOND WIRES PER PAD
GND PWR	2	-104	0	1
GND QUIET	1	0	0	1
COMP	3	-108	589	1
VS	4	-125	1350	1
DNC	5	-108	1452	1
DNC	6	1089	1452	1
DNC	7	1089	1350	1
VOUT SENSE	8	1072	598	1
VOUT FORCE	9	1088	1	1
TRIM	10	985	-25	1

NOTES:

12. Origin of coordinates is the centroid of GND QUIET.
13. Bond wire size is 1 mil.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
February 27, 2014	FN8451.3	On page 1, Under features: Added voltage accuracy over radiation with ±0.175% value.
February 10, 2014		On page 1: Under features changed the text from accuracy over temperature and radiation to: accuracy over temperature. "Pin Description" on page 2: Under description for pin number 4 added the lid connected to ground. Electrical specifications table for "Die" on page 5 under accuracy post rad updated min from -0.152 to -0.175 and max from +0.15 to +0.175.
September 13, 2013	FN8451.2	Electrical specifications table for Output Voltage (V_{OUT}) on page 4 and page 5: Removed VIN= 5V from conditions cell. Electrical specifications table for dropout voltage on page 4 and page 5: Changed VOUT = 2.5V @ 10mA to IOUT = 10mA. Electrical specifications table for "Flatpack" on page 4 as follow: Removed V_{OUT} = 2.5V from Input Voltage Range, Line Regulation, Dropout Voltage, Output Voltage Noise, Broadband Voltage Noise, Noise Density. Electrical specifications table for "Die" on page 5 as follow: Removed V_{OUT} = 2.5V from Input Voltage Range, Line Regulation, Dropout Voltage. Typical Performance Curves on page 6 added "COUT = 0.1µF, COMP = 1nF" to header.
September 4, 2013		Added C_{OUT} = 0.1µF, COMP = 1nF to Electrical spec table on page 5.
August 30, 2013		Added die sale part number to Electrical spec table on page 5. Added 1nF COMP to figure 1 on page 1. Electrical Spec on page 4: Changed I_{OUT} = 0 to I_{OUT} = 0mA. Added die sale part number to electrical spec table on page 5.
August 8, 2013	FN8451.1	Page 1, Related Literature. Updated title of AN1847 from "ISL71090SEH25 Evaluation Board User's Guide" to ""ISL71090SEHXX Evaluation Board User's Guide"
June 6, 2013	FN8451.0	Initial Release.

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

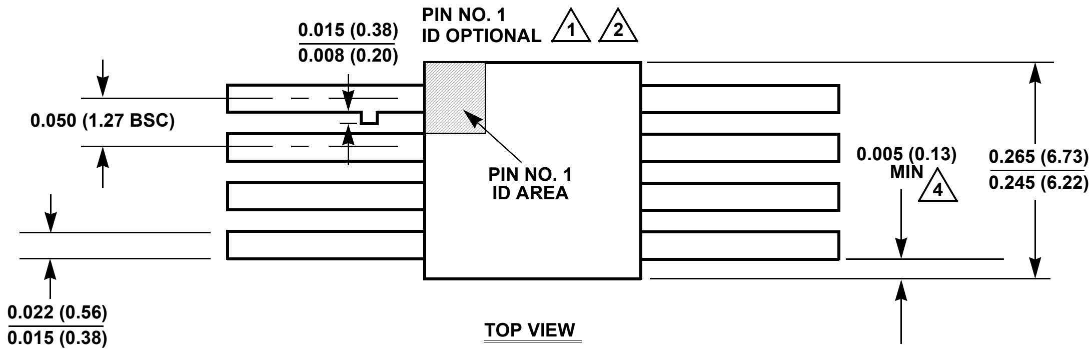
For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

Package Outline Drawing

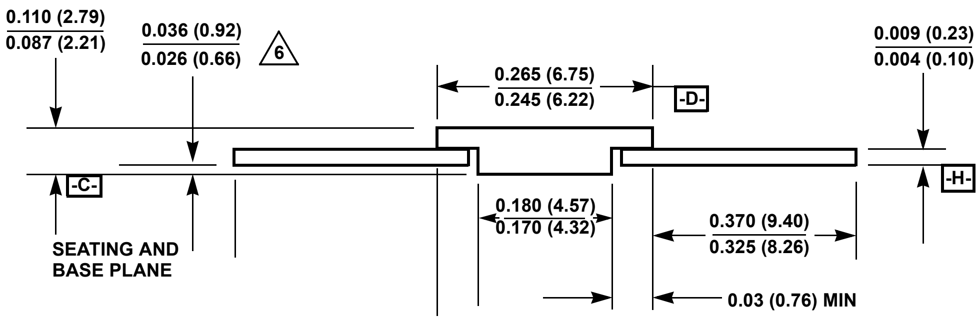
K8.A

8 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

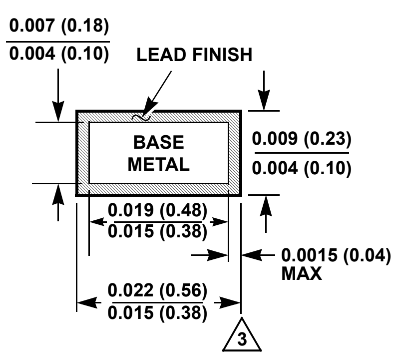
Rev 3, 3/13



TOP VIEW



SIDE VIEW



SECTION A-A

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.